

EXHIBIT M



US006292428B1

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Tomita et al.

(10) Patent No.: US 6,292,428 B1
(45) Date of Patent: Sep. 18, 2001

(54) SEMICONDUCTOR DEVICE RECONCILING DIFFERENT TIMING SIGNALS

(75) Inventors: Hiroyoshi Tomita; Tatsuya Kanda, both of Kawasaki (JP)

(73) Assignee: Fujitsu Limited, Kanagawa (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/240,007

(22) Filed: Jan. 29, 1999

(30) Foreign Application Priority Data

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(51) Int. Cl.⁷ G11C 8/00

(52) U.S. Cl. 365/233; 365/230.08; 365/189.05

(58) Field of Search 365/233, 230.08, 365/189.05, 240

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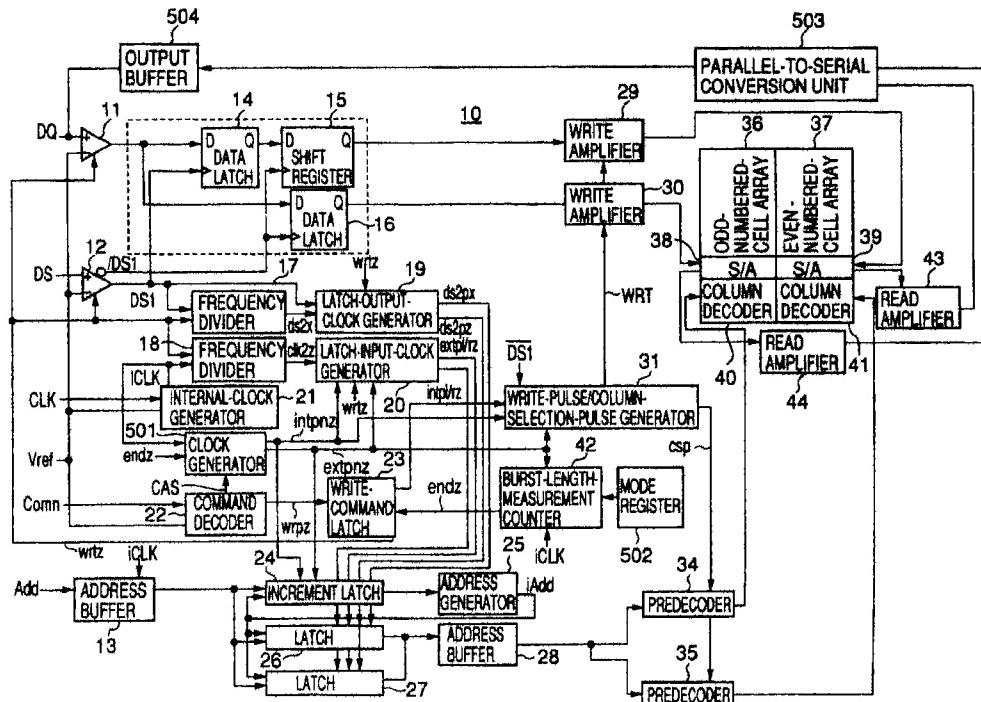
Primary Examiner—Huan Hoang

(74) Attorney, Agent, or Firm—Arent Fox Kintner Plotkin & Kahn, PLLC

(57) ABSTRACT

A semiconductor device which receives addresses in synchronism with a clock signal and receives data in synchronism with a strobe signal includes address-latch circuits, a first control circuit which selects one of the address-latch circuits in sequence in response to the clock signal, and controls the selected one of the address-latch circuits to latch a corresponding one of the addresses in response to the clock signal, and a second control circuit which selects one of the address-latch circuits in sequence in response to the strobe signal, and controls the selected one of the address-latch circuits to output a corresponding one of the addresses in response to the strobe signal.

42 Claims, 25 Drawing Sheets



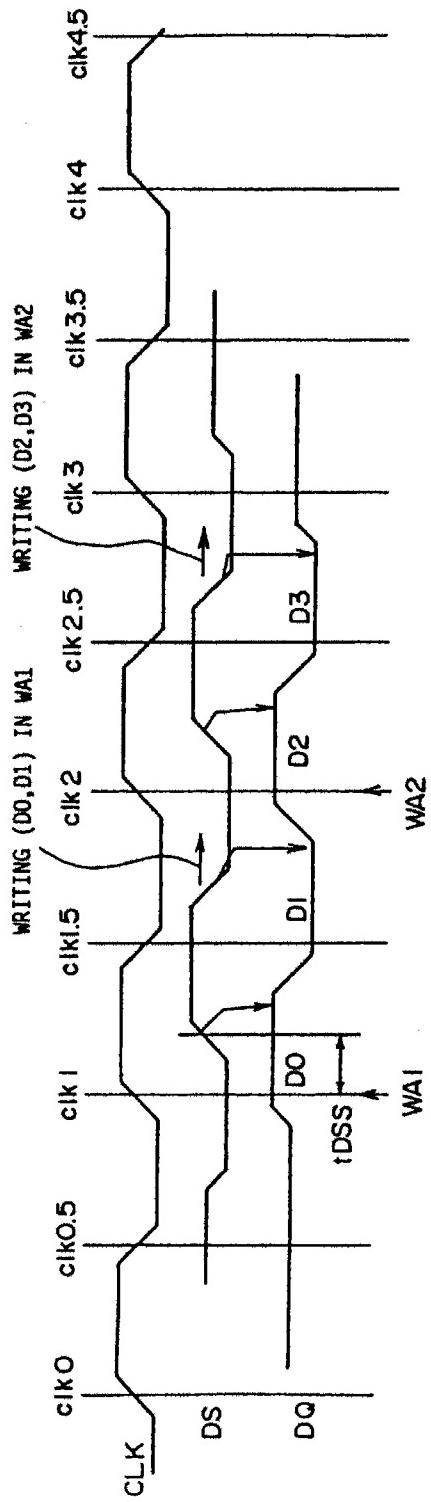
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FIG. 1



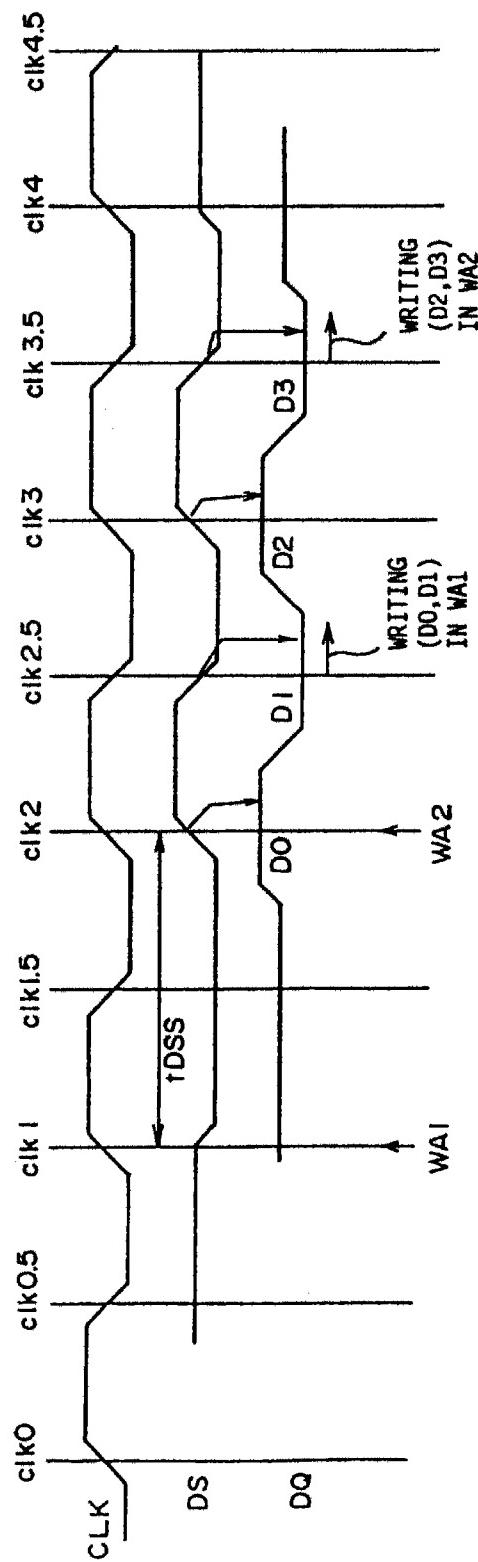
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FIG. 2



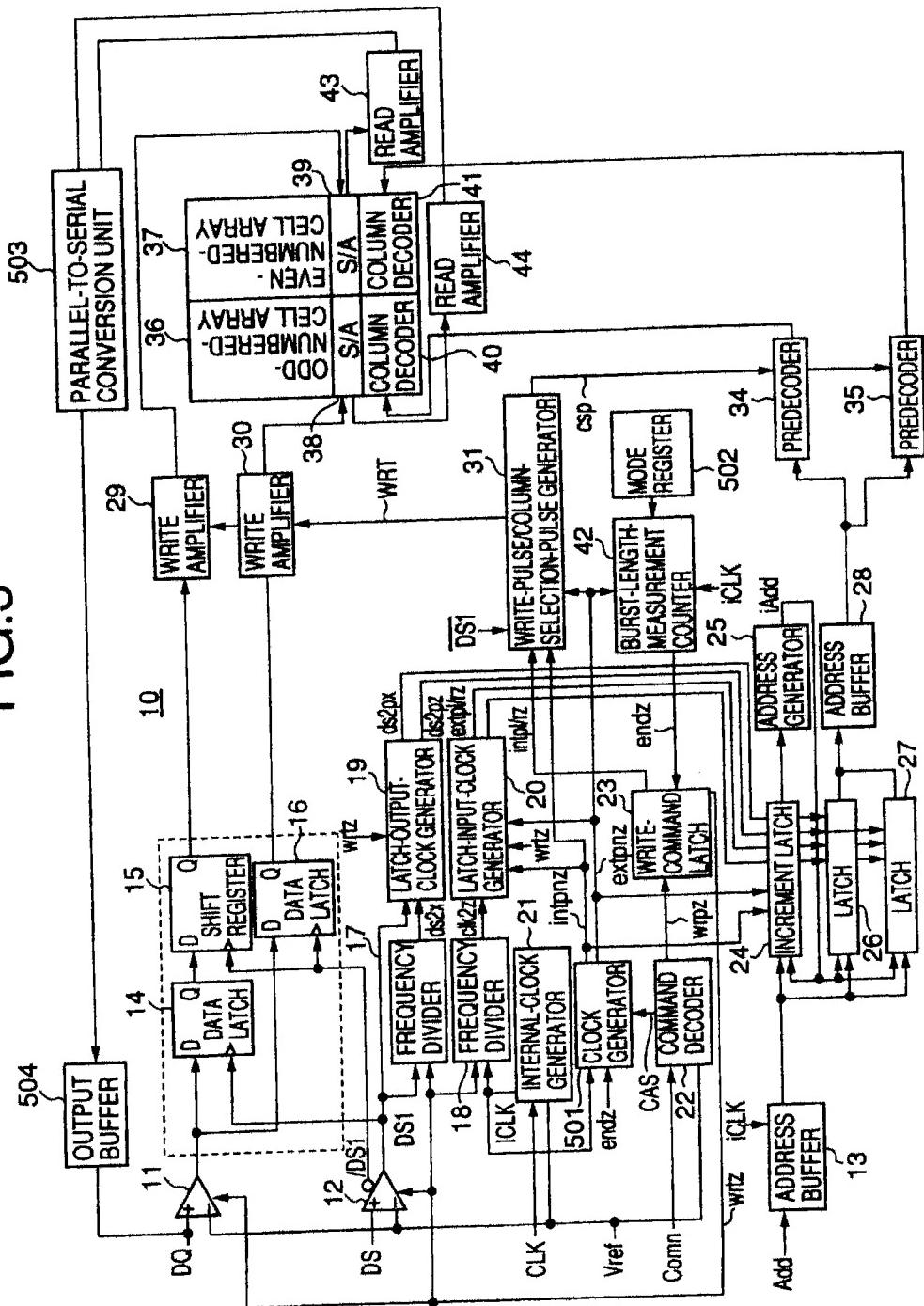
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FIG.3

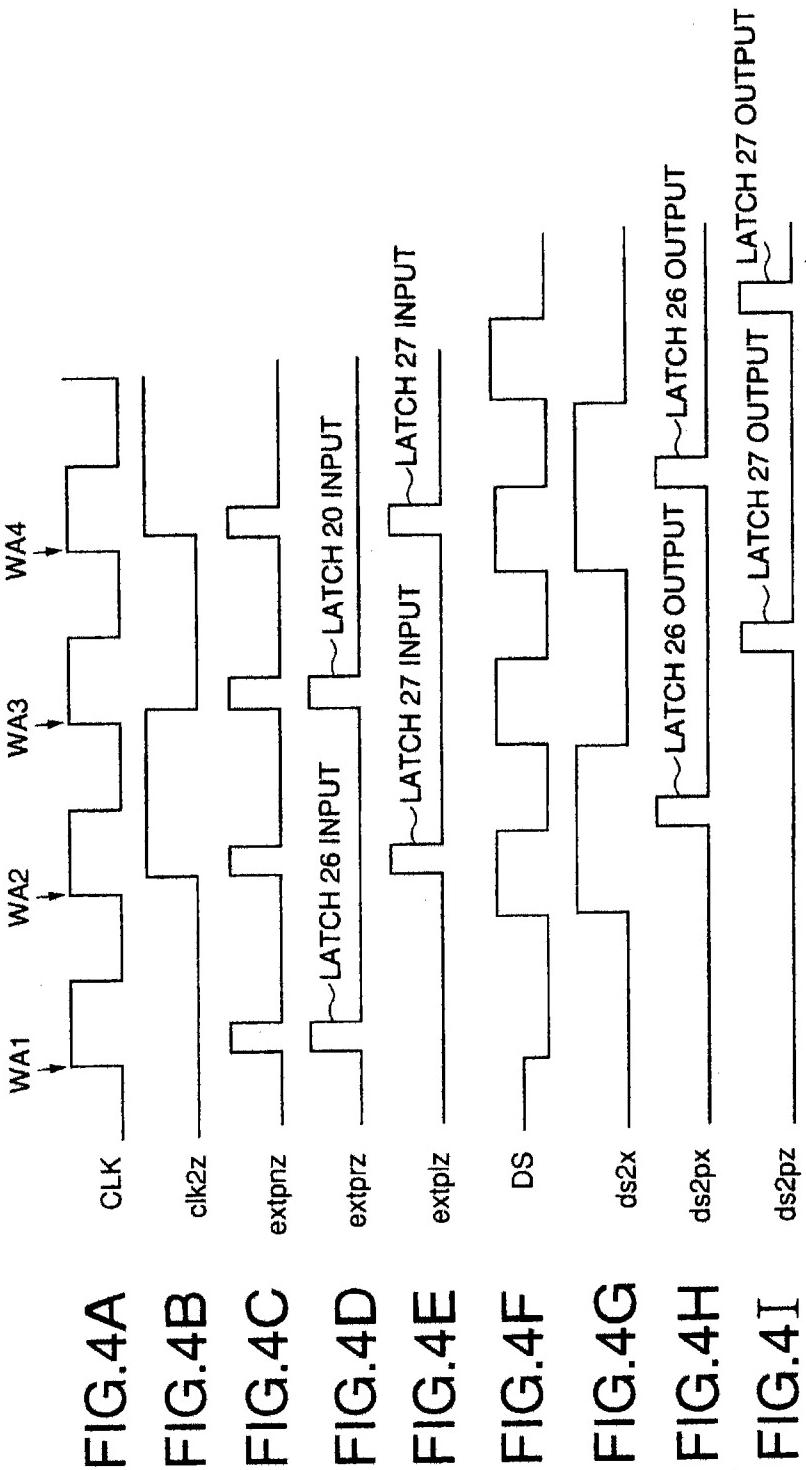


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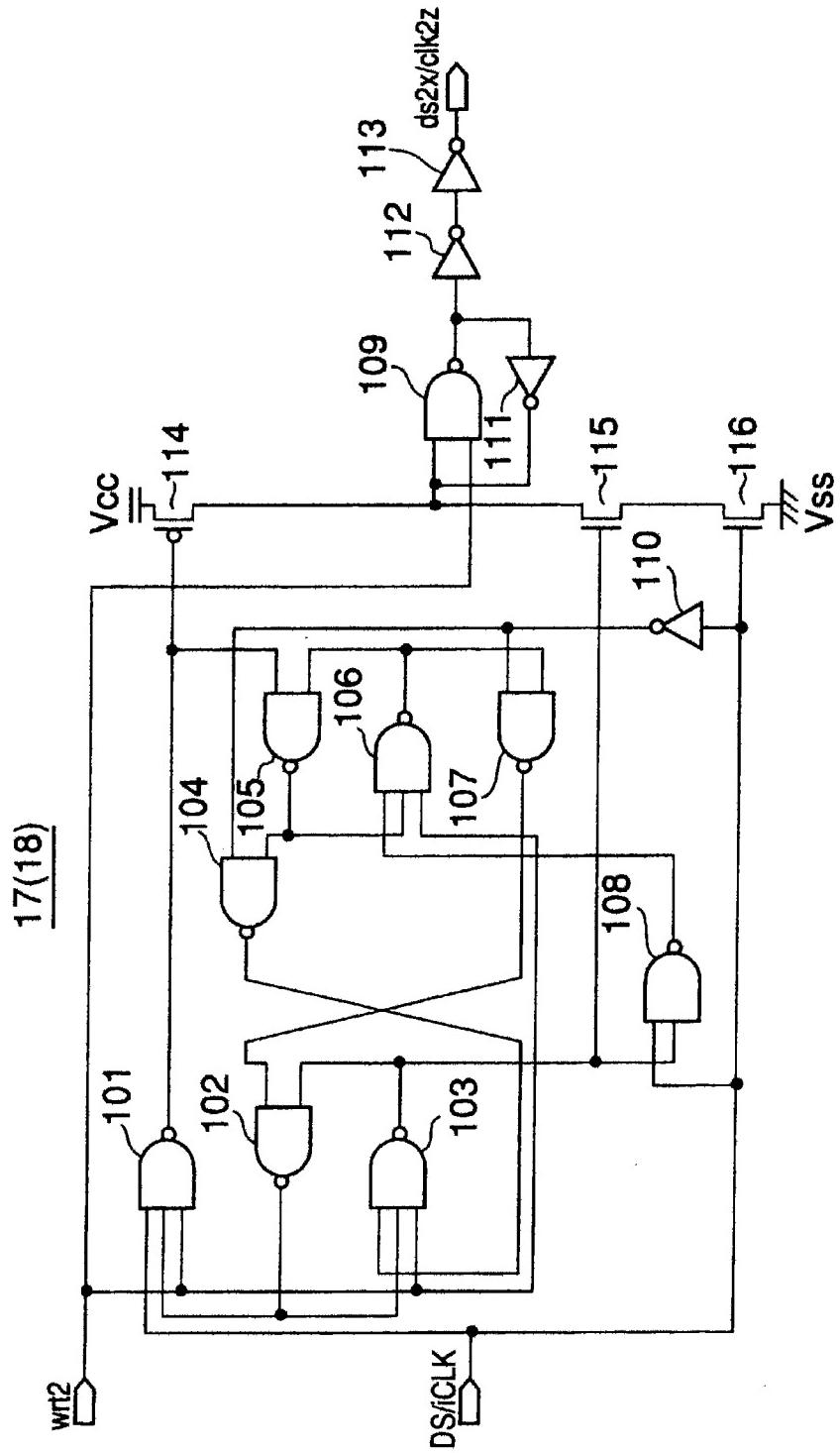
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FIG. 5



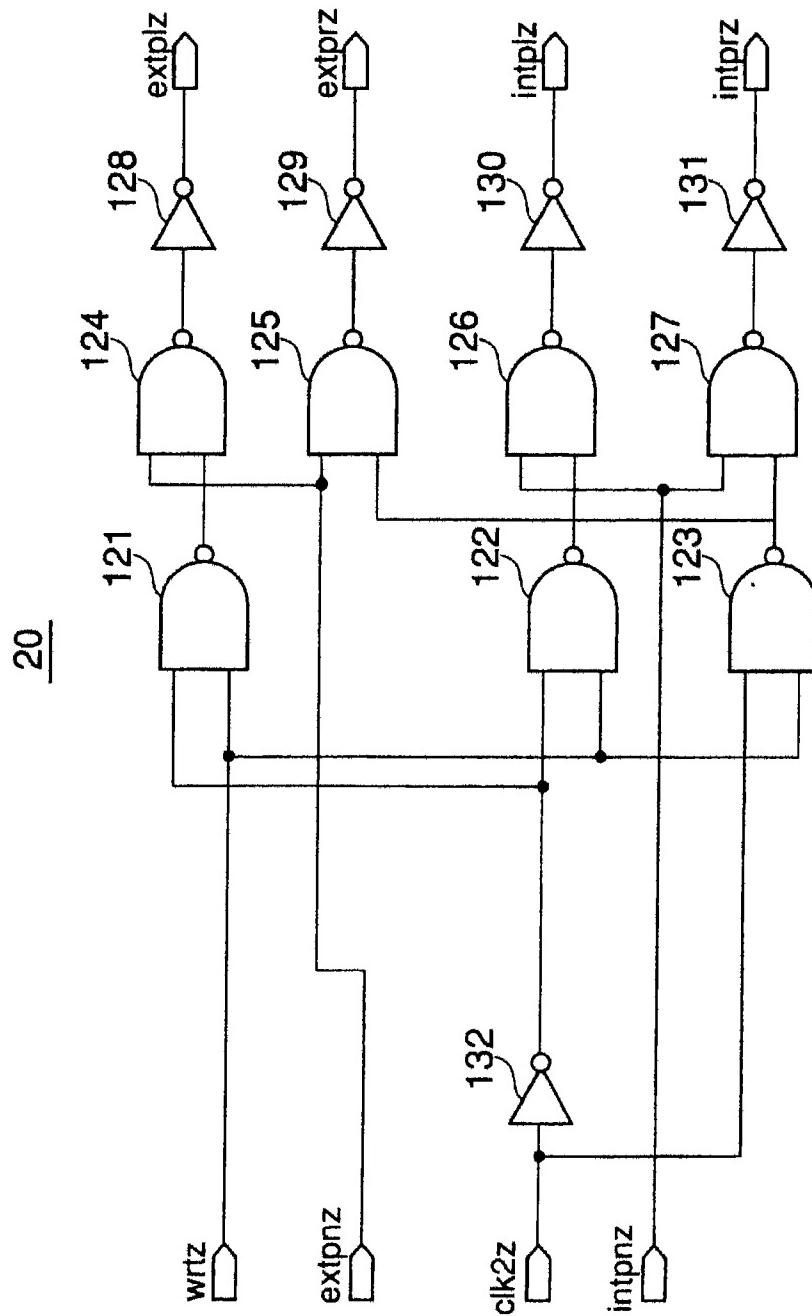
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FIG.6



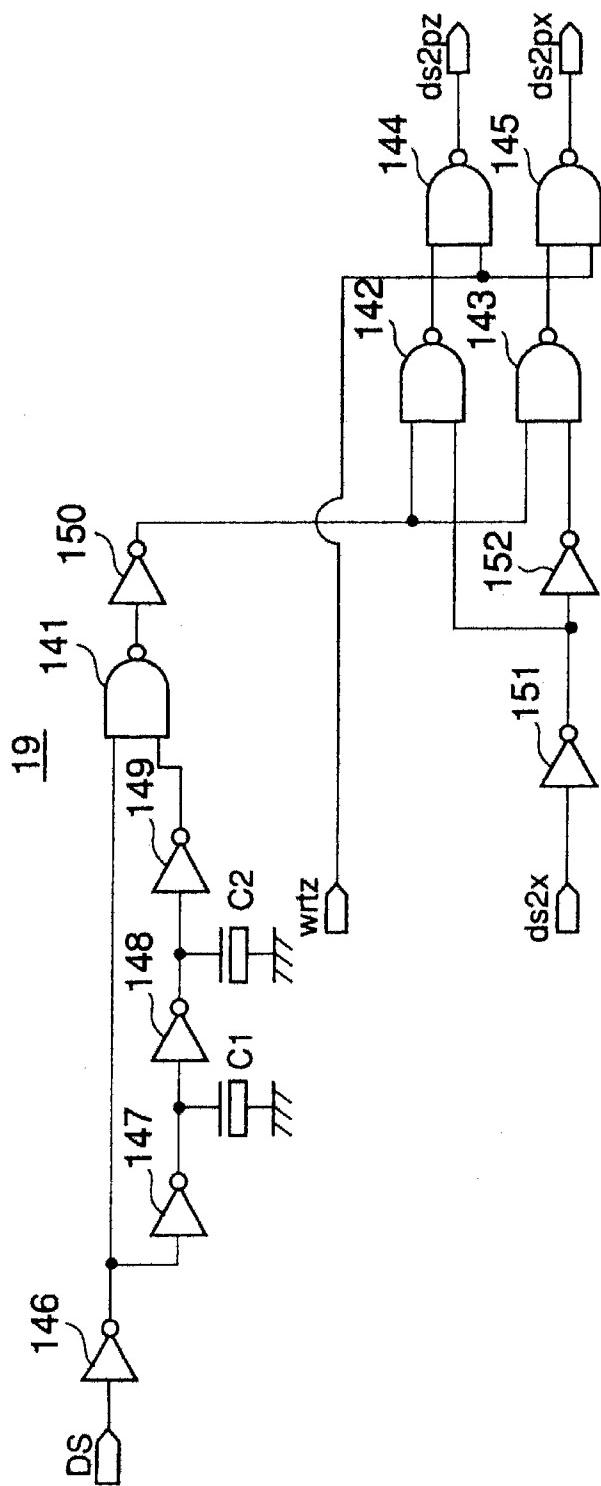
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FIG. 7



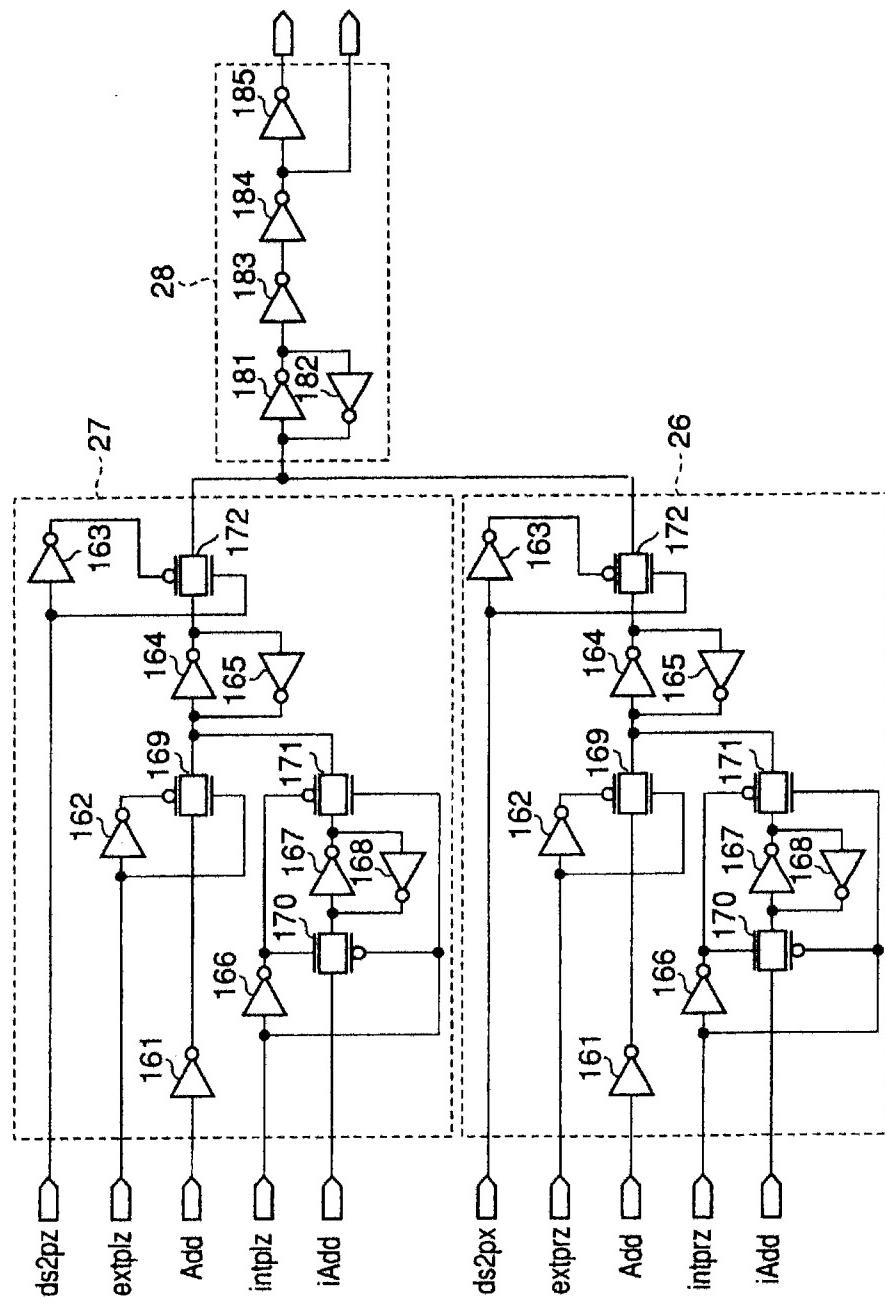
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FIG. 8



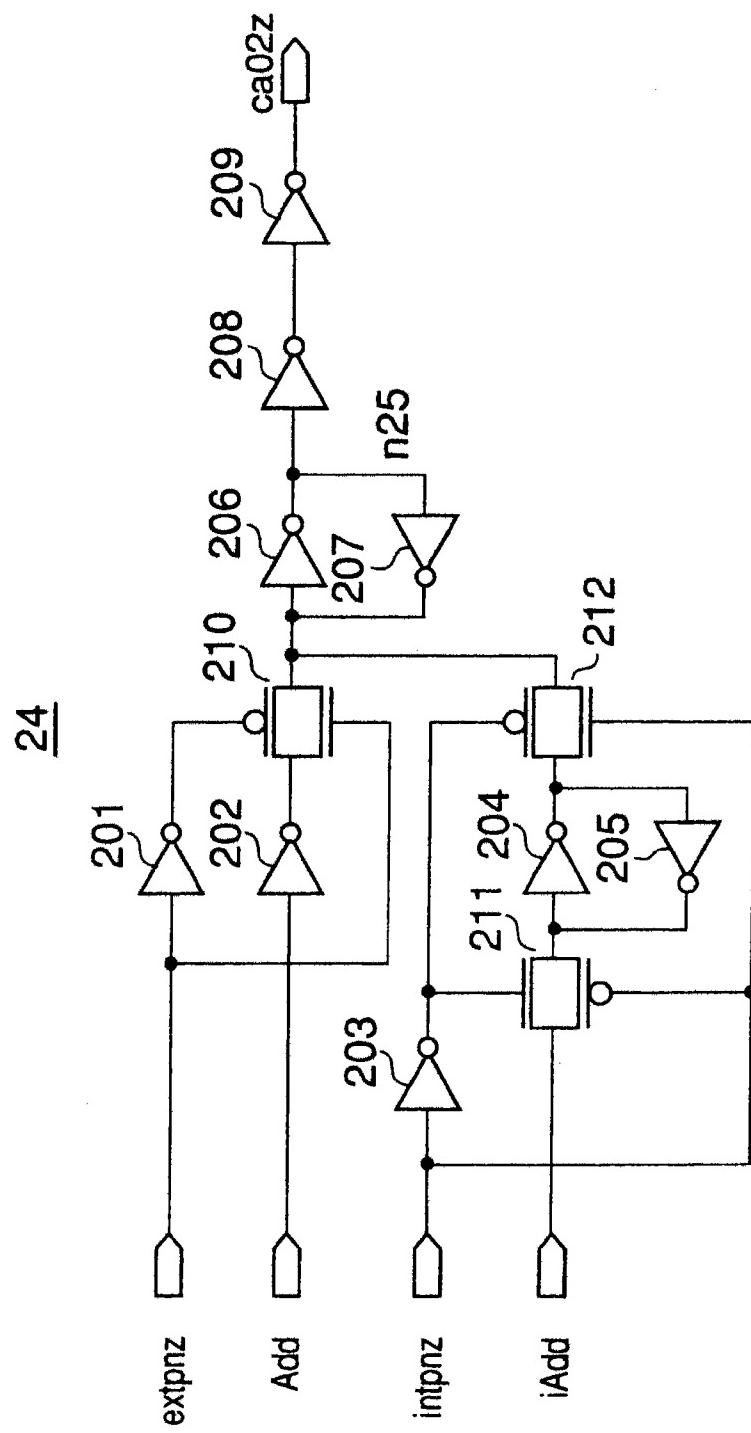
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FIG. 9



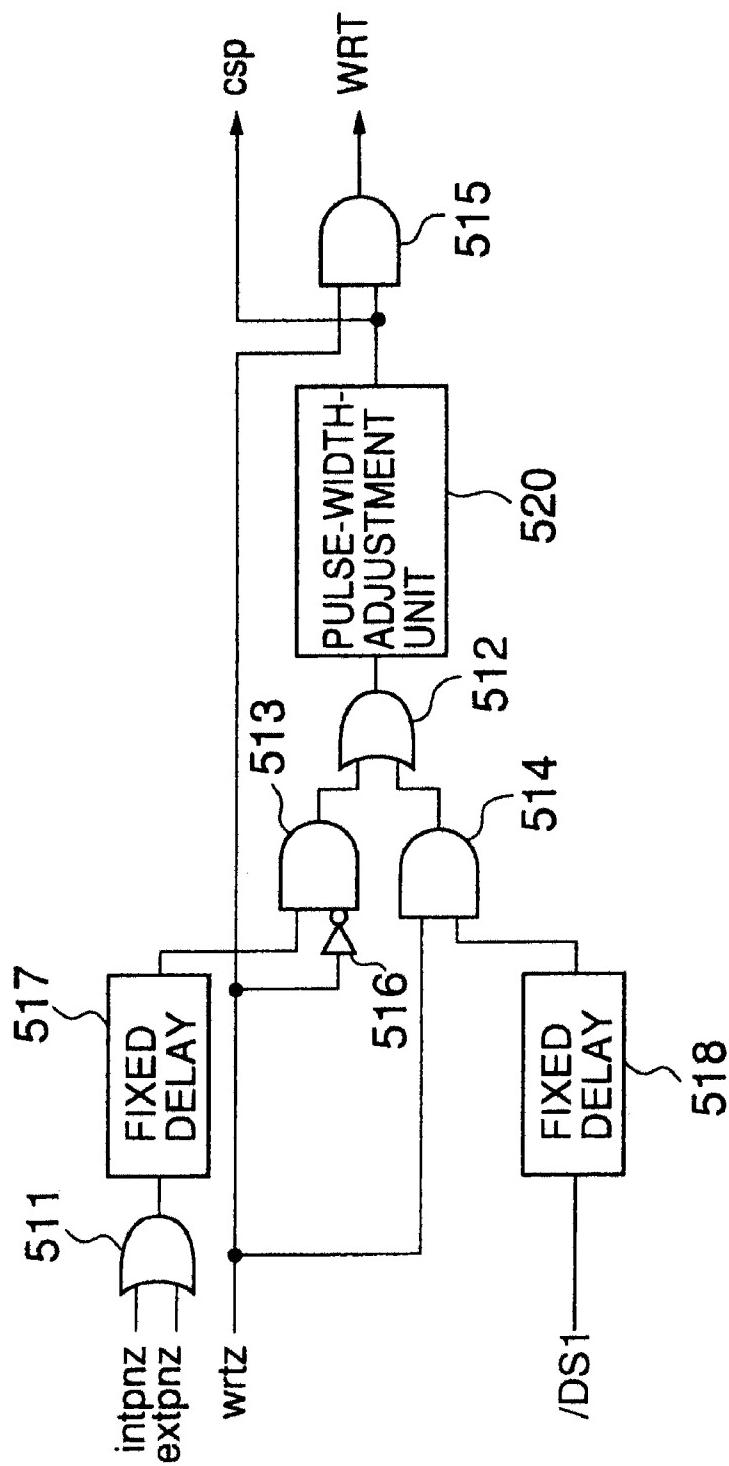
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FIG. 10

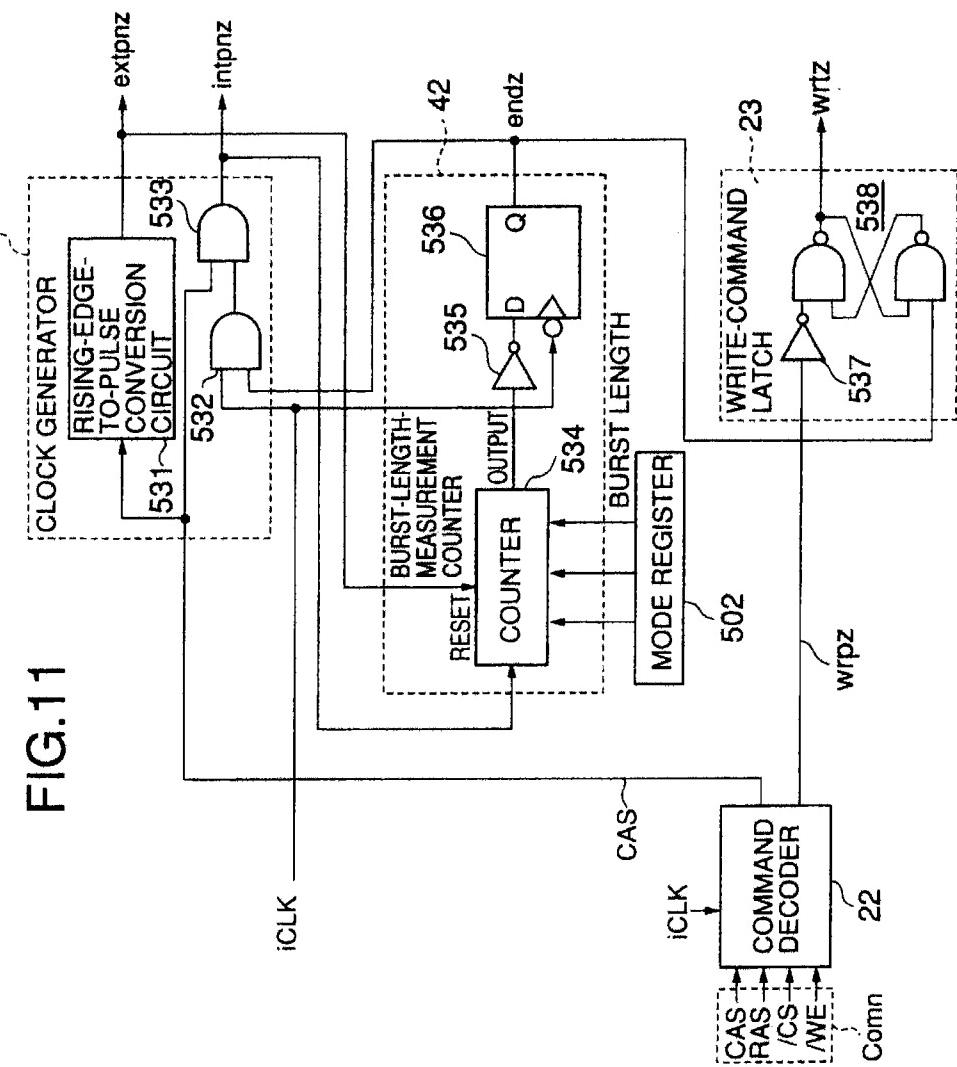


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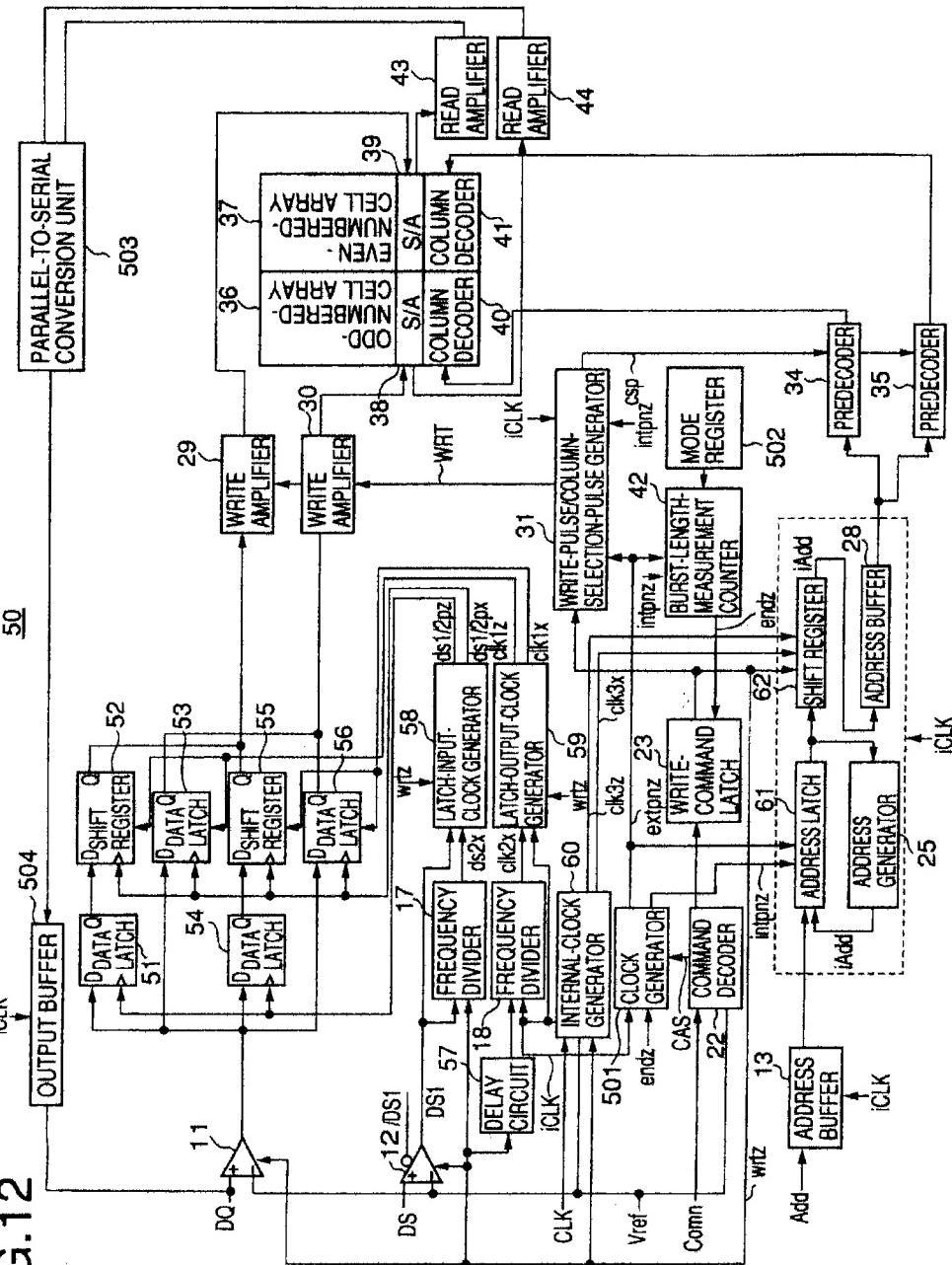
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FIG. 12



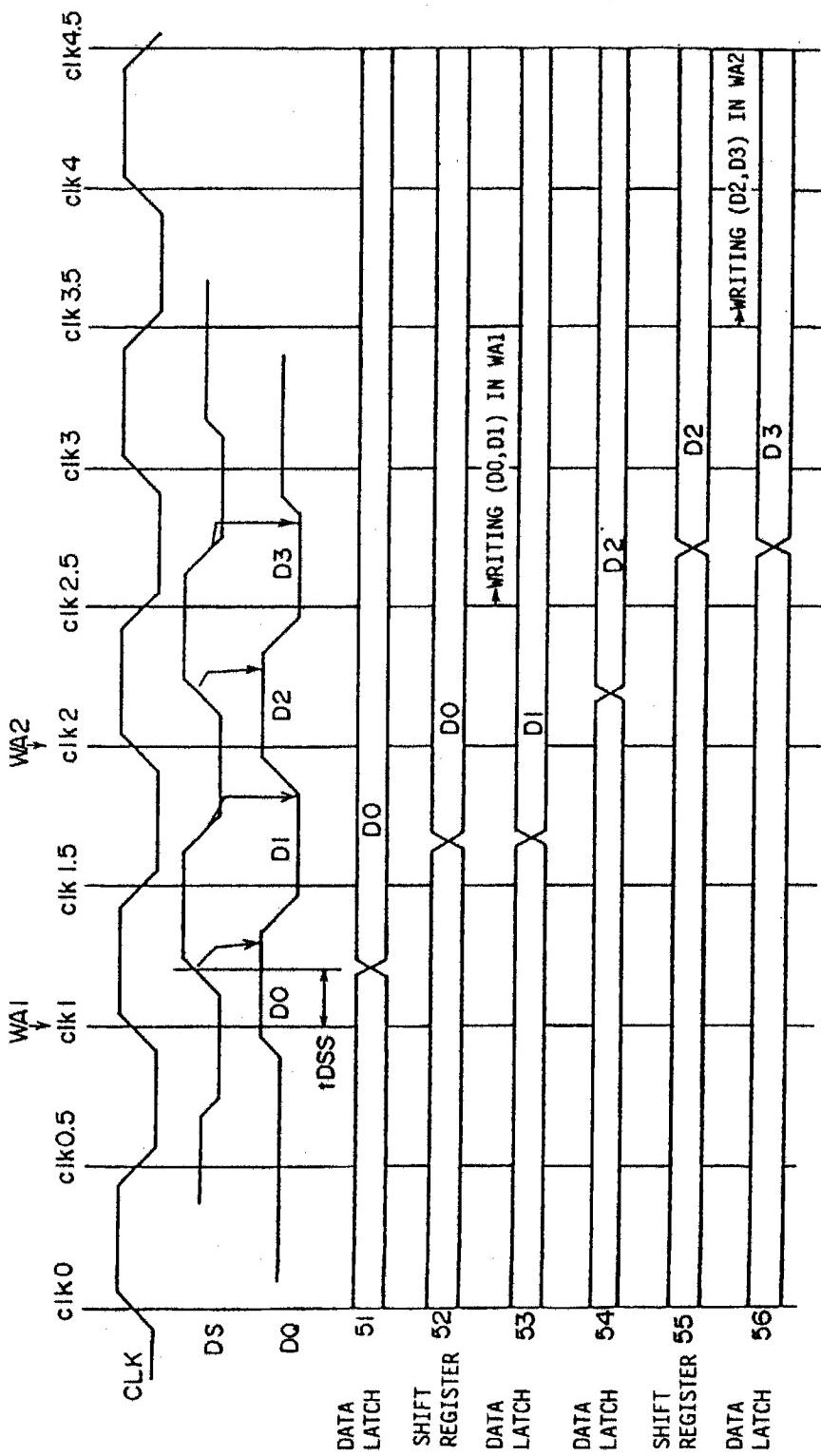
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FIG. 13



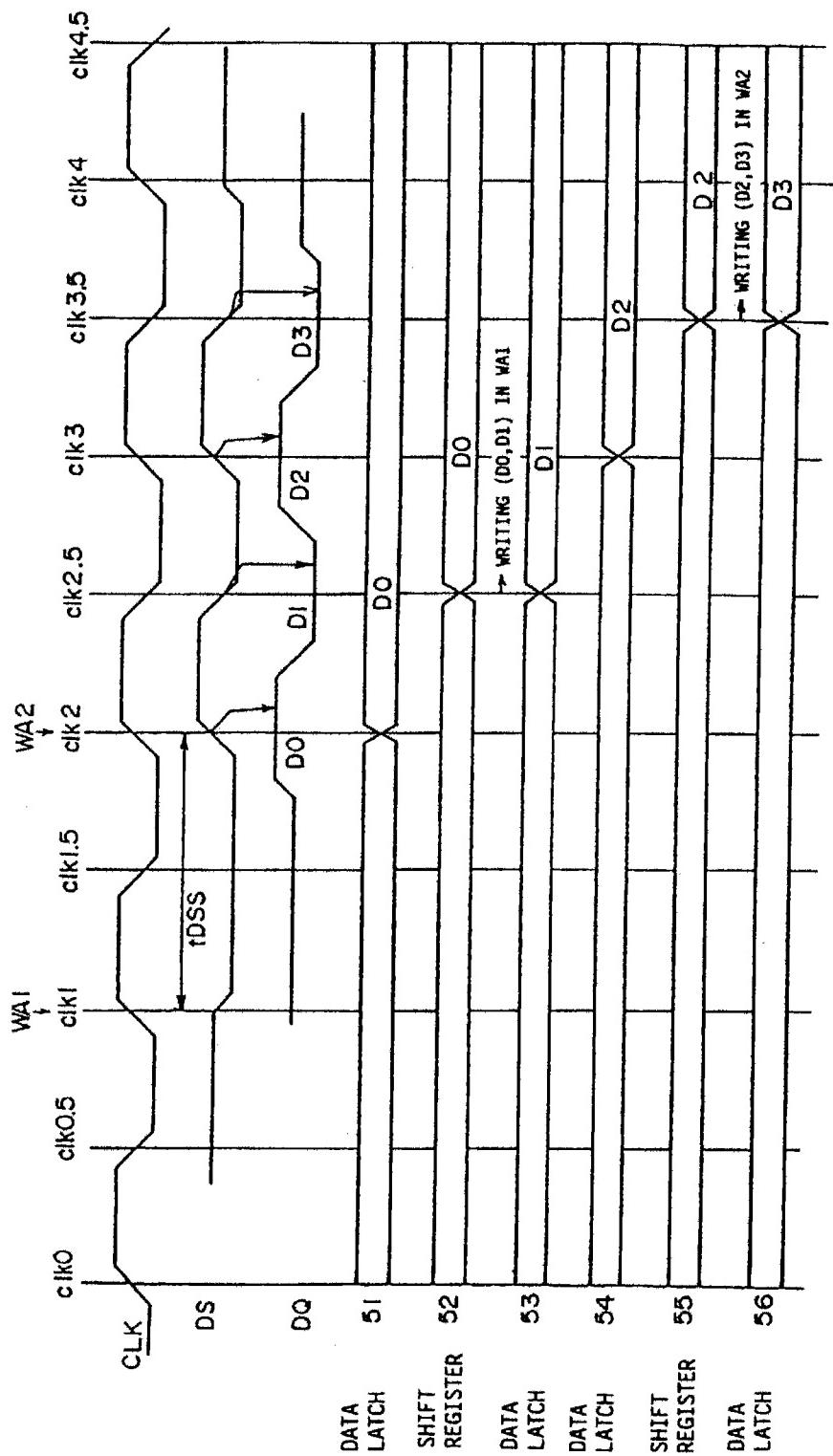
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FIG. 14



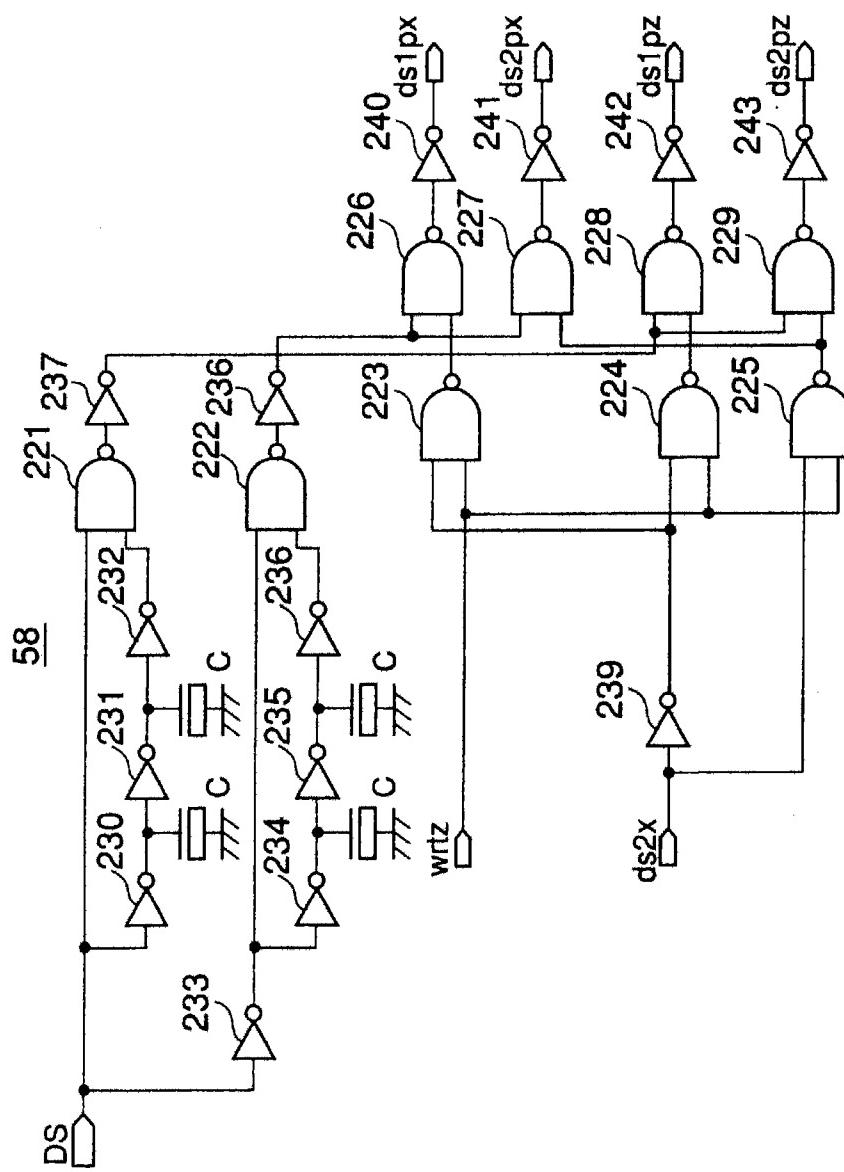
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FIG. 15



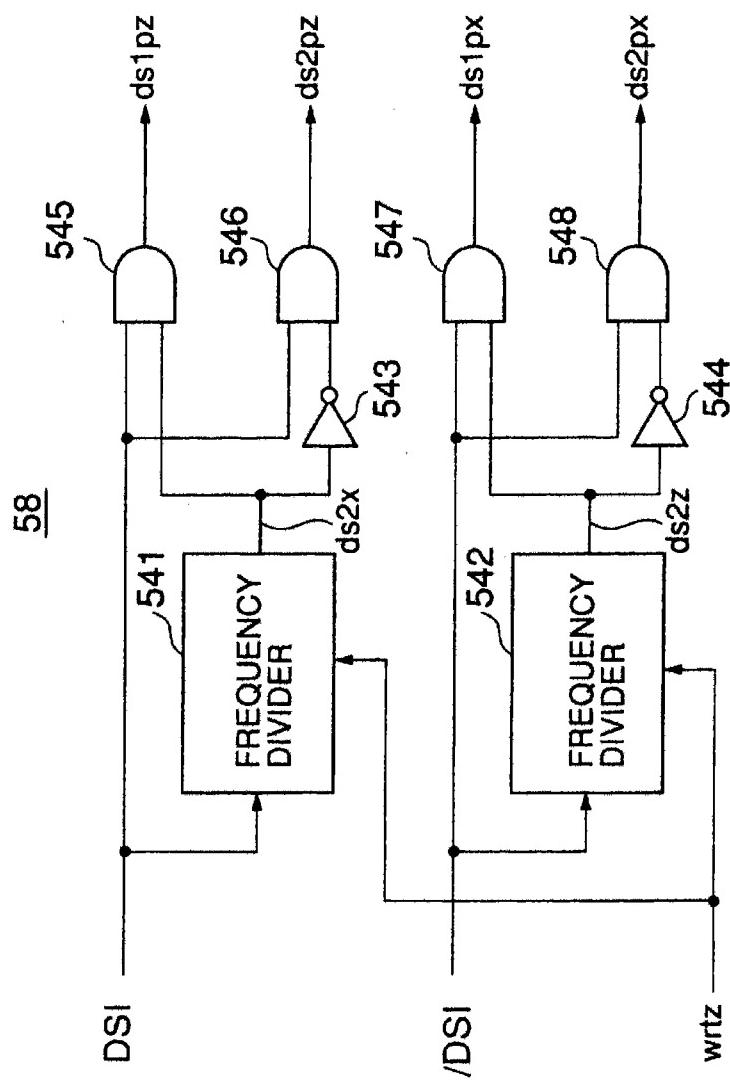
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FIG. 16



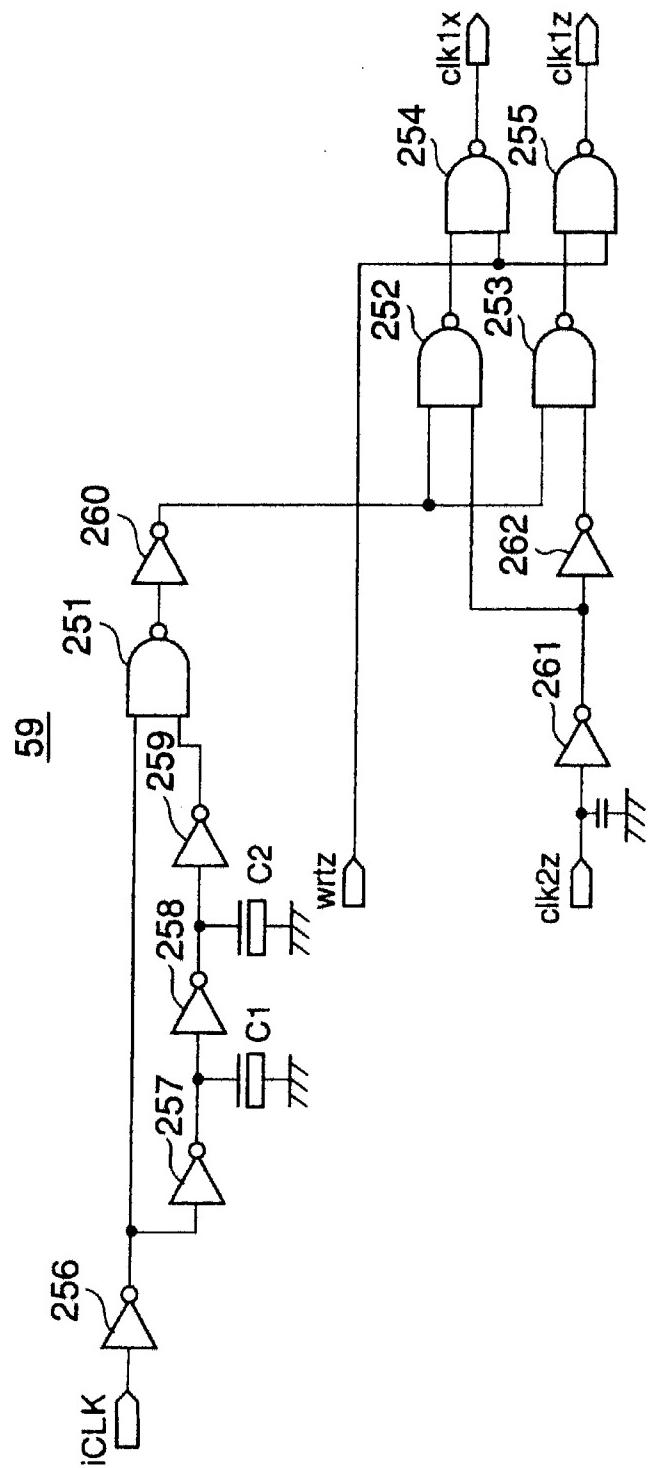
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FIG. 17



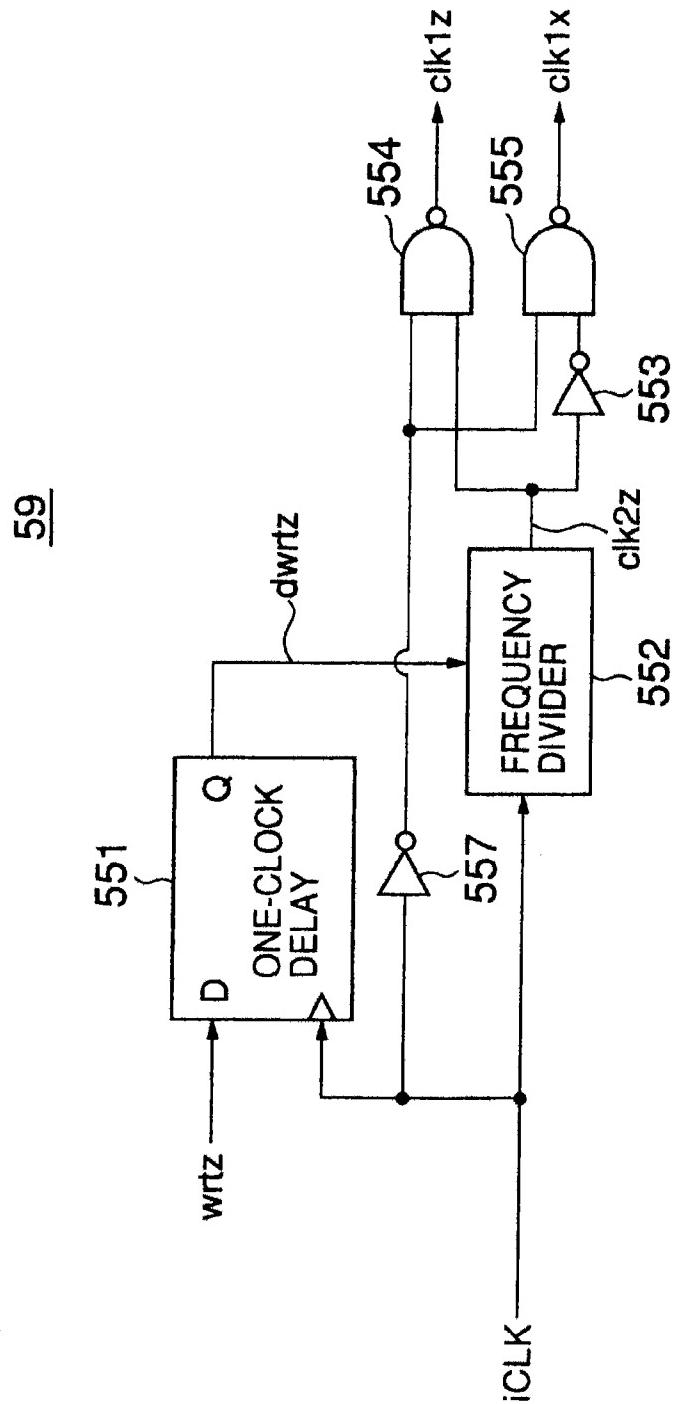
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FIG. 18



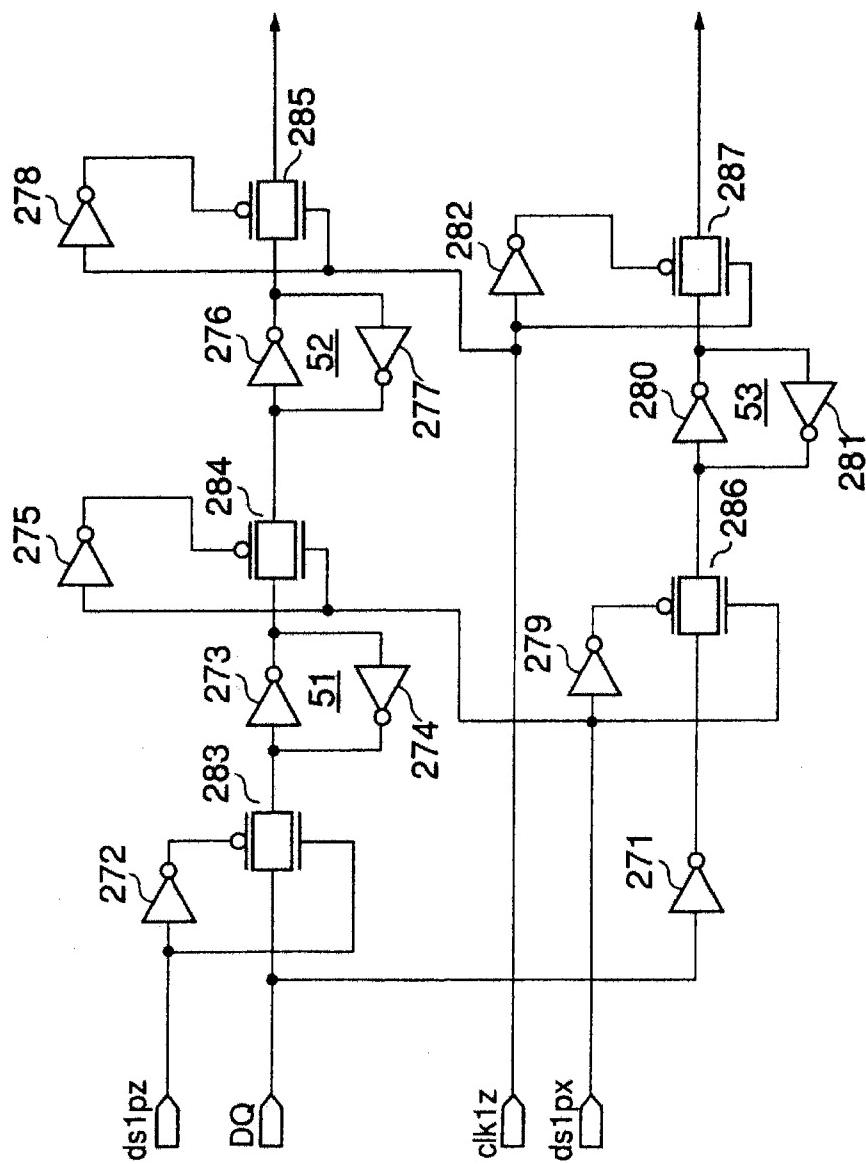
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FIG.19



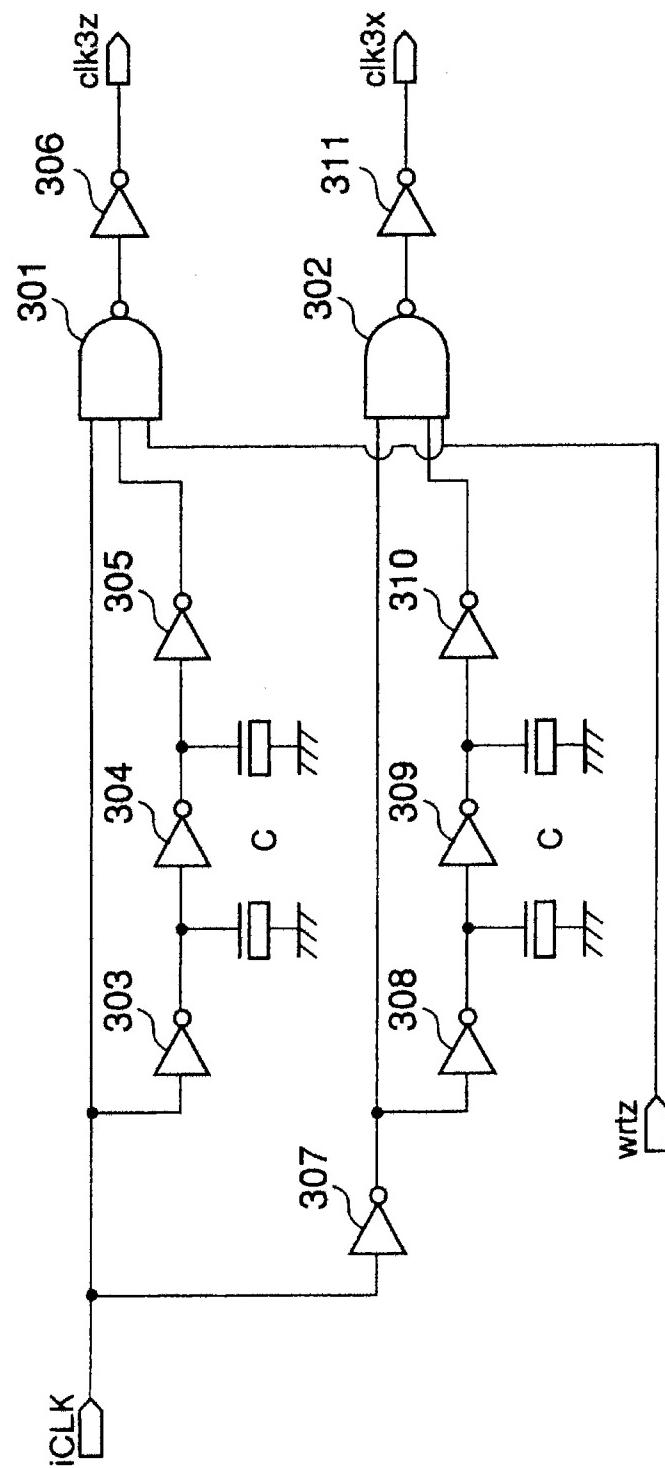
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FIG.20



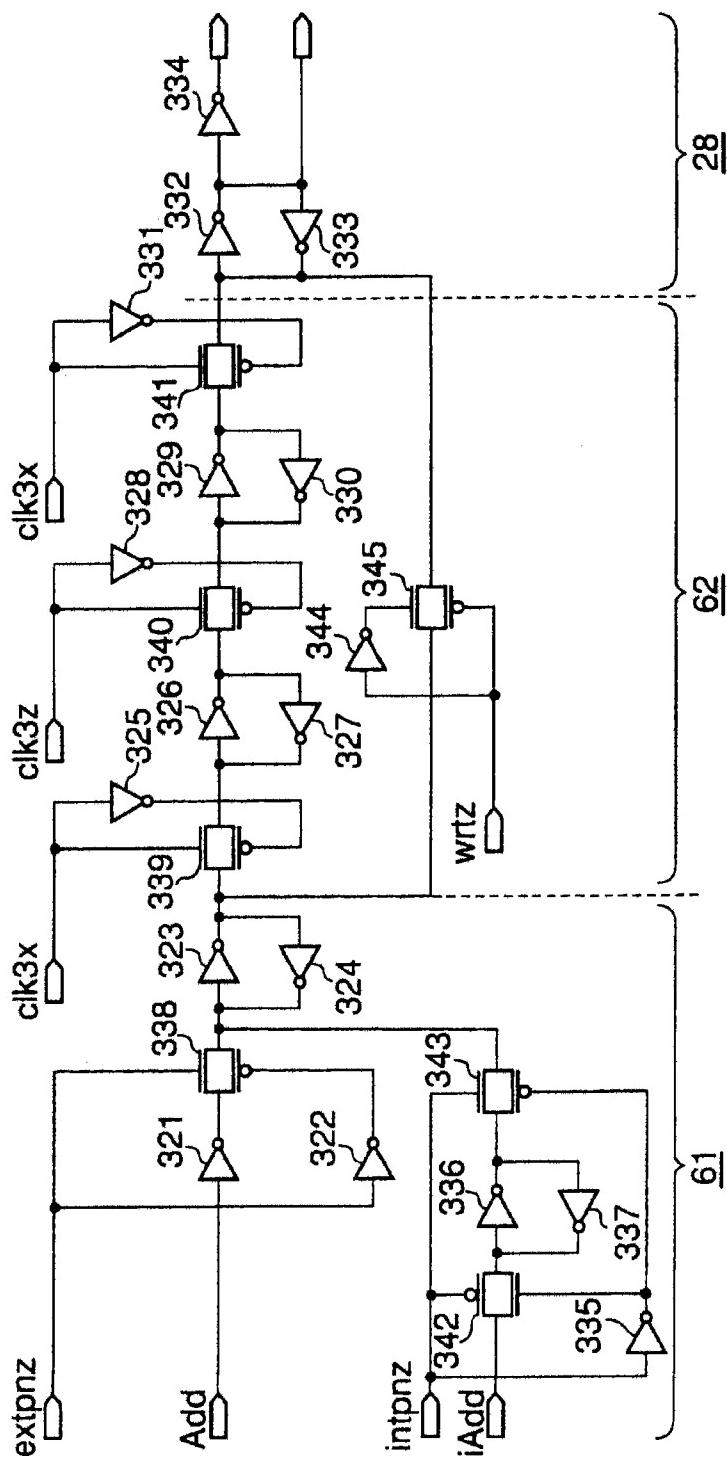
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FIG.21



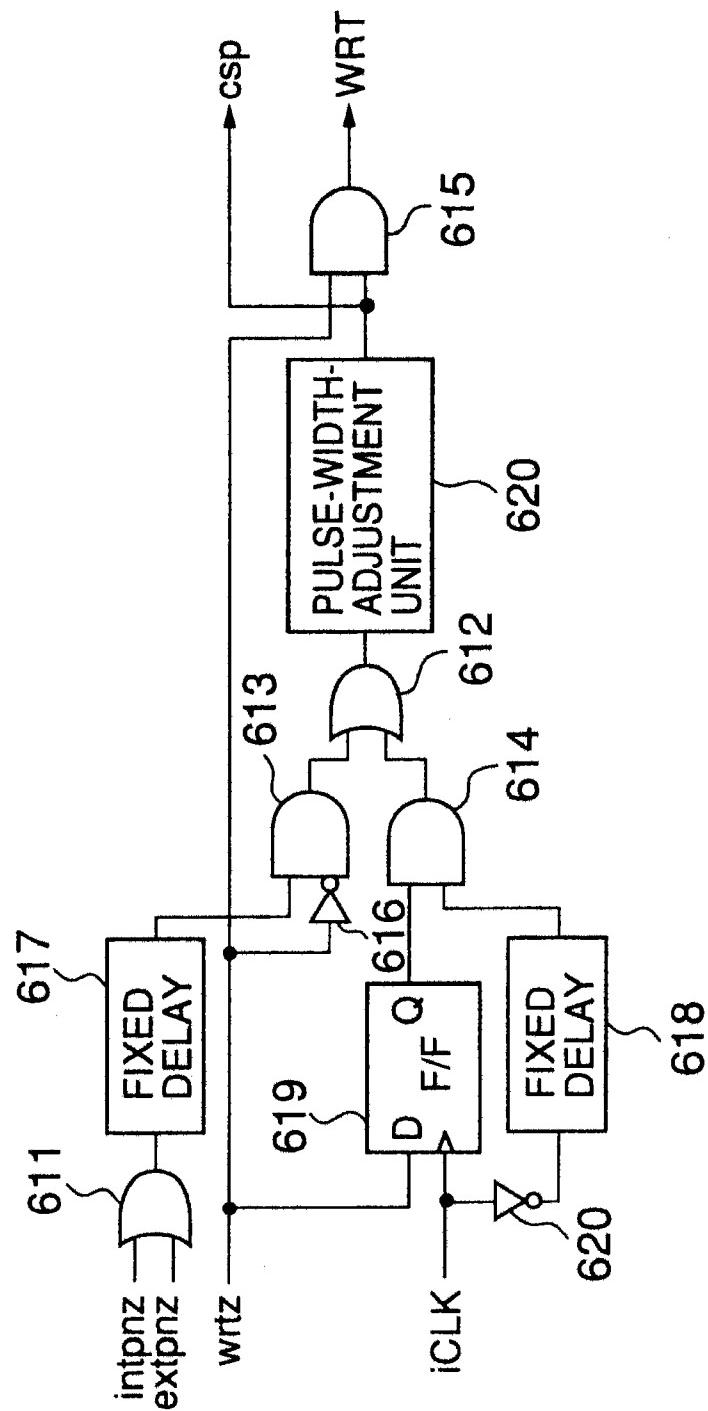
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FIG.22



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FIG.23

